

"FEE ADDRESS" INDICATION FORM

To: MAIL STOP: M Fee Correspondence
U.S. Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Please recognize as the "Fee Address," under the provisions of 37 CFR 1.363, the following address:


COMPUTER PATENT ANNUITIES, INC.
225 Reinekers Lane
Suite 400
Alexandria, VA 22314

Payor Number: 000197

in the following listed application(s) or patent(s) for which the issue fee has been paid.

<u>Patent No.</u>	<u>Serial No.</u>	<u>Patent Date</u>	<u>US Filing Date</u>	<u>Confirmation No.</u>	<u>Attorney Docket No.</u>
7,554,117B2	10/809,118	6/30/09	3/25/04	7733	0553-0404

Respectfully Submitted,



Mark J. Murphy
Registration No. 34,225
Date: August 28, 2009

COOK ALEX Ltd.
200 West Adams Street
Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Customer No: 26568



US007554117B2

(12) United States Patent
Nakamura**(10) Patent No.: US 7,554,117 B2**
(45) Date of Patent: Jun. 30, 2009

- (54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**
- (75) Inventor: **Osamu Nakamura, Atsugi (JP)**
- (73) Assignee: **Semiconductor Energy Laboratory Co., Ltd. (JP)**
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 841 days.

5,739,890 A 4/1998 Uda et al.
 5,754,263 A 5/1998 Akiyama et al.
 5,757,054 A 5/1998 Miyawaki et al.
 5,767,827 A 6/1998 Kobayashi et al.
 5,910,271 A 6/1999 Ohe et al.
 5,933,204 A 8/1999 Fukumoto
 5,946,561 A 8/1999 Yamazaki et al.
 5,949,107 A 9/1999 Zhang

(21) Appl. No.: **10/809,118**

(Continued)

(22) Filed: **Mar. 25, 2004****FOREIGN PATENT DOCUMENTS**

(65) **Prior Publication Data**
 US 2007/0181945 A1 Aug. 9, 2007

EP 0 349 255 B1 12/1997

(30) **Foreign Application Priority Data**
 Mar. 26, 2003 (JP) 2003-086425

(Continued)

OTHER PUBLICATIONS

- (51) Int. Cl. **H01L 29/04** (2006.01)
H01L 31/036 (2006.01)
- (52) U.S. Cl. **257/72; 257/347; 257/E29.117**
- (58) Field of Classification Search **257/59, 257/72, 347, E27.112, E29.117**
- See application file for complete search history.

International Search Report (Application No. PCT/JP2004/003715; PCT/7064), Dated Jun. 8, 2004 (In Japanese).

(Continued)

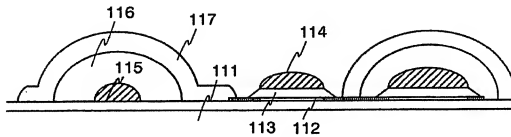
Primary Examiner—Hoi V Pham
(74) Attorney, Agent, or Firm—Cook Alex Ltd.

(56) **References Cited**
U.S. PATENT DOCUMENTS

(57) **ABSTRACT**

5,117,299 A 5/1992 Kondo et al.
 5,132,248 A 7/1992 Drummond et al.
 5,132,676 A 7/1992 Kimura et al.
 5,155,564 A 10/1992 Hishida et al.
 5,210,050 A 5/1993 Yamazaki et al.
 5,240,801 A 8/1993 Hayashi et al.
 5,330,616 A 7/1994 Yamazaki
 5,583,369 A 12/1996 Yamazaki et al.
 5,592,318 A 1/1997 Majima et al.
 5,643,826 A 7/1997 Ohtani et al.
 5,652,667 A 7/1997 Kurogane
 5,706,067 A 1/1998 Colgan et al.

An island-like interlayer insulating film is formed selectively in a region where a source interconnection and a gate interconnection intersect. For example, by use of ink jet method, a solution containing an insulating material is dropped on a region where the gate interconnection and the source interconnection intersect or a region where a holding capacitor is formed, that enable to reduce a photolithography process and to reduce the number of masks that are used in a TFT.

18 Claims, 7 Drawing Sheets

(intersection of interconnections)

(TFT)

(holding capacitor)